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Characteristics of $Pt/SrTiO_3/Pb(Zr_{0.52}, Ti_{0.48})O_3/SrTiO_3/Si$ ferroelectric gate oxide structure

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Abstract

$Pt/SrTiO_3/Pb(Zr_{0.52}, Ti_{0.48})O_3/SrTiO_3/Si$ (MIFIS) ferroelectric gate oxide structures were prepared by an r.f. sputtering method for application of non-destructive read out ferroelectric RAM (NDRO-FRAM) devices. In the MIFIS structure, a $SrTiO_3$ (STO) film was used as a buffer layer to prevent the interaction between the $Pb(Zr_{0.52},Ti_{0.48})O_3$ (PZT) film and the Si substrate and also between the PZT film and the Pt top electrode. In the PZT/Si structure, a serious inter-diffusion of Pb into Si substrate was observed by Auger electron spectrometry (AES). However, STO/PZT/STO/Si structures had a perfect perovskite phase and a flat interface of PZT/STO/Si without the inter-diffusion of Pb into the Si substrate. When Pt/STO/PZT/STO/Si structures were post-annealed at 400°C for 30 min after depositing the Pt top electrodes, the leakage current of MIFIS structure was improved to about 10^{-8} A/cm^2. The property of the memory window of MIFIS structures was improved due to a low leakage current. When Pt/STO(25 nm)/PZT(160 nm)/STO(25 nm)/Si structures were annealed at 600°C for 1 h and post-annealed at 400°C for 30 min, the maximum value of the memory window was about 2 V at the applied voltage of 7 V. The memory window was increased as increasing the thickness of PZT film since a higher voltage was applied to the thicker PZT film.

Keywords: Ferroelectric gate oxide; MIFIS structure; Memory window; Non-destructive read out ferroelectric RAM

1. Introduction

Recently, non-volatile ferroelectric memory devices (NVFRAM) have been widely researched. NDRO (non-destructive read out)-FRAM devices [1–3] are composed of only one transistor which use ferroelectric thin films as gate oxides [4,5]. In addition, the stored data is not destroyed after read-out process and the rewrite process is not demanded. These properties are similar to EEPROM (electrically erasable programmable ROM) devices. Generally, EEPROM devices need a high operating voltage, usually 10 V, and have low rewrite cycles (about 10^4×). However, NDRO-FRAMs have a low operating voltage (less than 5 V) and high rewrite cycles (more than 10^{10}×). Therefore, NDRO-FRAM is a candidate device for the application of a non-volatile memory device due to the simple structure of one transistor and a low operating voltage, and a long recycle time. In order to realize a NDRO-FRAMs, metal/ferroelectric/semiconductor (MFS) structures have been proposed but it had serious problems such as the inter-diffusion between the ferroelectrics and the semiconductor and formation of interfacial layers [6]. In this work, metal/insulator/ferroelectric/insulator/ semiconductor (MIFIS) structures have been proposed using double buffer layers above and below the PZT film. The $Pt/SrTiO_3/Pb(Zr,Ti)O_3/SrTiO_3/Si$ structures were prepared by an r.f.-sputtering method and the electrical properties and the micro-structures of MIFIS structures were characterized.

2. Experimental

$Pb(Zr,Ti)O_3$ (PZT) and $SrTiO_3$ (STO) films were prepared on p-Si (100) substrates by an r.f. magnetron sputtering method. The following Table 1 is the conditions of depositing PZT and STO films. STO/PZT/STO/Si structures were annealed at 600°C for 1 h in oxygen ambient in order to obtain the PZT films with the perovskite structure. Pt top electrodes were deposited by a d.c. sputtering at the room temperature. After depositing Pt top electrodes, Pt/STO/PZT/STO/Si structures were post-annealed at 400°C for 30 min in oxygen ambient. The crystallinity and composition of PZT and STO films were characterized, respectively,

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Table 1
Sputtering conditions of PZT and STO films preparation

Target materials	$SrTiO_3$	$Pb(Zr_{0.52}, Ti_{0.48})O_3$
Substrate	p-Si (100).	
Base pressure of system (Torr)	3×10^{-6}	
Sputtering pressure (Torr)	2×10^{-2}	
RF power (W)	40	80
Gas ratio ($Ar:O_2$)	1:1	
Substrate temperature (°C)	500	300

by X-ray diffraction (XRD) and electron probe mass analysis (EPMA). The surface and interface of Pt/STO/PZT/STO/Si structures was observed by scanning electron microscope (SEM) and transmission electron microscope (TEM), respectively. The depth profiles of PZT/Si and STO/PZT/STO/Si structures were analyzed by Auger electron spectrometry (AES) in order to observe the inter-diffusion at the interface. The electrical properties of Pt/STO/PZT/STO/Si gate structures were characterized by current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements, respectively.

3. Results and discussion

Fig. 1 shows the XRD patterns of the PZT/Si, the STO/Si, and the STO/PZT/STO/Si structures deposited with the conditions of Table 1. Fig. 1a shows that the STO film was polycrystalline with the (200) preferred orientation. Fig. 1b,c show the XRD patterns of the PZT/Si and the STO/PZT/STO/Si structures annealed at 600°C for 1 h in oxygen ambient. As shown in Fig. 1b, the pyrochlore PZT phase was mainly formed in the PZT/Si structure without inserting a STO buffer layer due to the inter-diffusion of Pb atoms into the Si substrate. However, in case of the STO/PZT/STO/Si structure as shown in Fig. 1c, the PZT film had a perfect perovskite structure. In addition, the inter-diffusion of the PZT/Si and the STO/PZT/STO/Si structures were analyzed by AES depth profiles as shown in Fig. 2. A serious diffusion of Pb atoms into the Si substrate was observed in the PZT/Si structure as shown in Fig. 2a and a SiO_2 layer seemed to be formed between the PZT and the Si substrate. From these results, the pyrochlore PZT phase in the PZT/Si structure might be induced by the deficiency of Pb due to the penetration of Pb atoms into the Si substrate. This means that the PZT/Si structure was not suitable for the application of a ferroelectric gate oxide transistor due to the instability of the interface reaction. On the other hand, for AES depth profile in the STO/PZT/STO/Si structure as shown in Fig. 2b, the diffusion of Pb atoms was nearly not observed since the STO buffer layer could prevent efficiently Pb atoms from diffusing into the Si substrate. The surface and interface images of the Pt/STO/PZT/STO/Si structures were observed by SEM and TEM, respectively. Fig. 3 shows the surface photographs of the PZT/Si and the STO/PZT/STO/Si structures. The surface of the PZT/Si

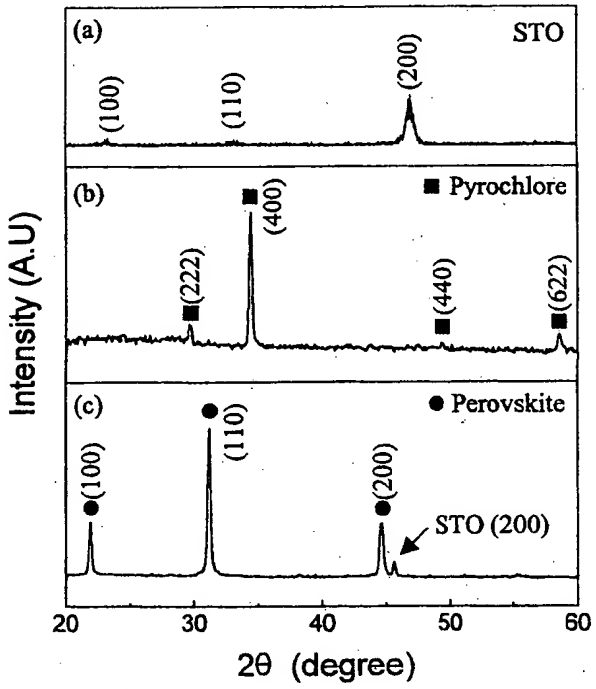

Fig. 1. XRD data of (a) STO/Si, (b) PZT/Si, and (c) STO/PZT/STO/Si structures annealed at 600°C for 1 h in oxygen ambient.

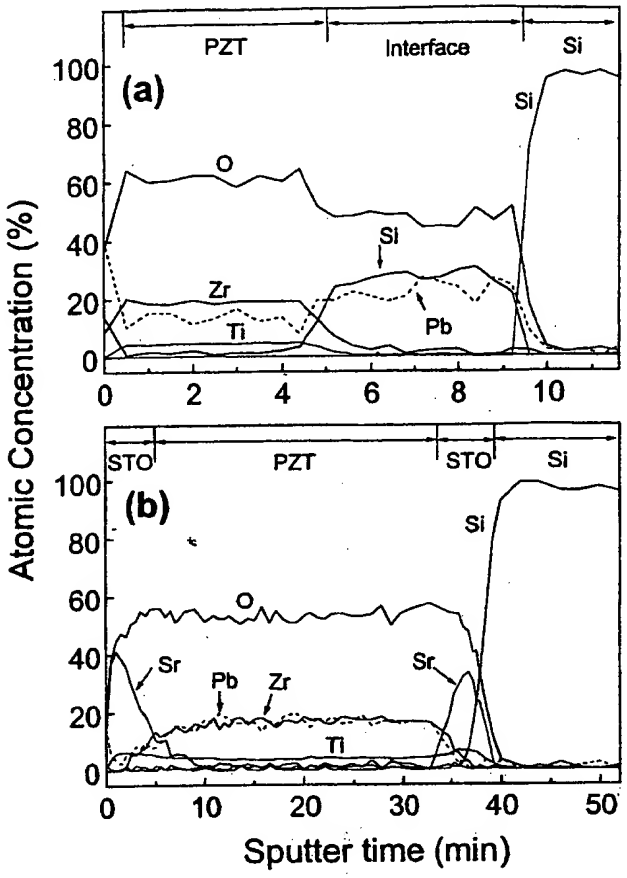

Fig. 2. AES depth profile of (a) PZT/Si and (b) STO/PZT/STO/Si structures annealed at 600°C for 1 h in oxygen ambient.

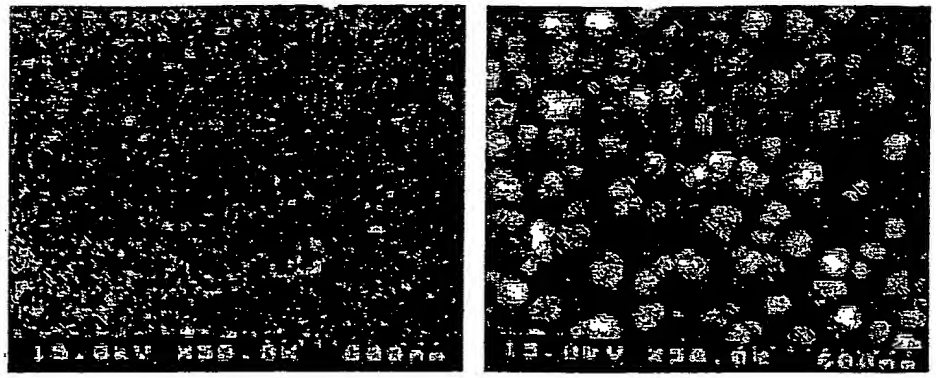

Fig. 3. SEM images of the surface of (a) PZT/Si and (b) STO/PZT/STO/Si structures annealed at 600°C for 1 h in oxygen ambient.

structure as shown in Fig. 3a revealed that the grains of the PZT film could be not sufficiently grown because of the inter-diffusion of Pb atoms as shown in the AES result (see Fig. 2b). However, the grains of the PZT film in the STO/PZT/STO/Si structure as shown in Fig. 3b had a larger grain size than in the PZT/Si structure. In addition, the interface of Pt/STO/PZT/STO/Si structure was observed by TEM as shown in Fig. 4. The STO film between the Pt top electrode and the PZT film seemed to be amorphous phase as shown in Fig. 4a. This STO film contacted directly to the Pt top electrode could decrease the interaction of Pt and PZT film. The interface of the PZT/STO/Si structure was fairly flat and clear and 5 nm thick SiO_2 layer was formed between the STO and the Si substrate during the annealing process. Therefore, it was concluded that the STO film was a good diffusion barrier between the PZT and the Si substrate or Pt electrode.

The electrical properties of the Pt/STO/PZT/STO/Si (MIFIS) structures were characterized by *C–V* and *I–V* measurements. Fig. 5 shows the *C–V* characteristics of the Pt/STO(25 nm)/PZT(160 nm)/STO(25 nm)/Si structures with different annealing processes. The STO/PZT/STO/Si structure as shown in Fig. 5a was annealed at 600°C for 30 min in oxygen ambient and then the Pt top electrode was deposited. The capacitance in the accumulation region near zero voltage was partially increased due to a high leakage current and the capacitance was relatively small due to a imperfect crystallization of the PZT film. Fig. 5b shows that the *C–V* curve of the STO/PZT/STO/Si structure annealed at 600°C for 1 h in oxygen ambient. The memory window of the MIFIS structure was about 0.4 V at the applied voltage of 5 V as the Pt-top electrode was not post-annealed. On the other hand, when the STO/PZT/STO/Si structure was annealed at 600°C for 1 h and the Pt/STO/PZT/STO/Si structure was post-annealed at 400°C for 30 min in oxygen ambient. The value of memory window was increased from 0.4 V to 1.2 V as shown in Fig. 5c. This improvement of memory window might be caused by the decrease of the defects or vacancies formed during the deposition of the Pt top electrode [7]. Fig. 6 shows the *I–V* characterization of the samples as shown in Fig. 5a–c. When the MIFIS structure was annealed at 600°C for 1 h and post-annealed at 400°C for 30 min in oxygen ambient, the leakage current density became to decrease to 10^{-8} A/cm^2 as shown in Fig. 6c. From above results, it could be seen that a high leakage

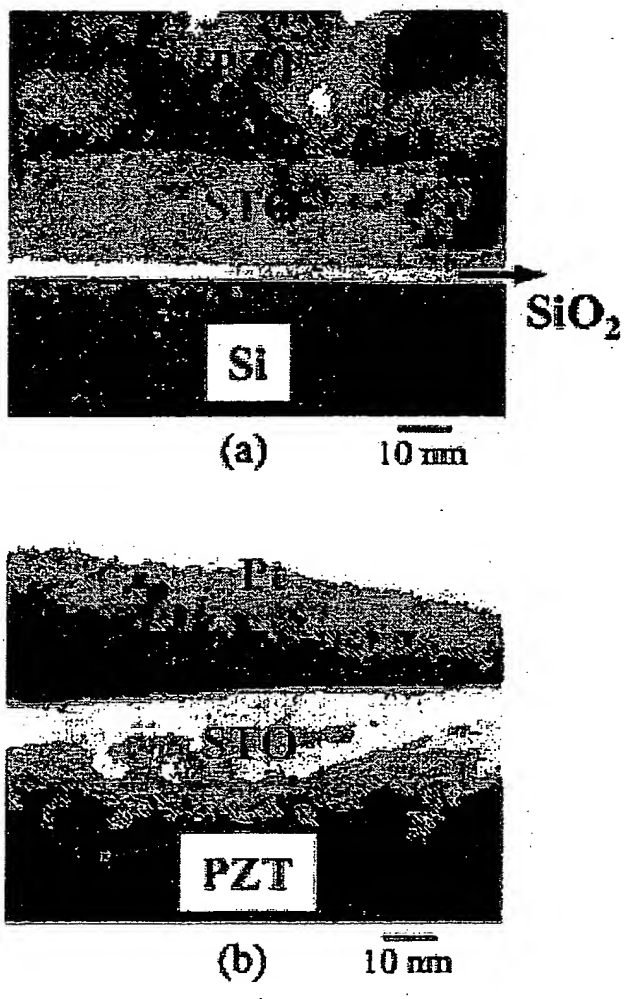

Fig. 4. TEM the cross sectional views of (a) PZT/STO/Si and (b) Pt/STO/PZT interfaces at Pt/STO/PZT/STO/Si structure annealed at 600°C for 1 h and post-annealed at 400°C for 30 min in oxygen ambient.

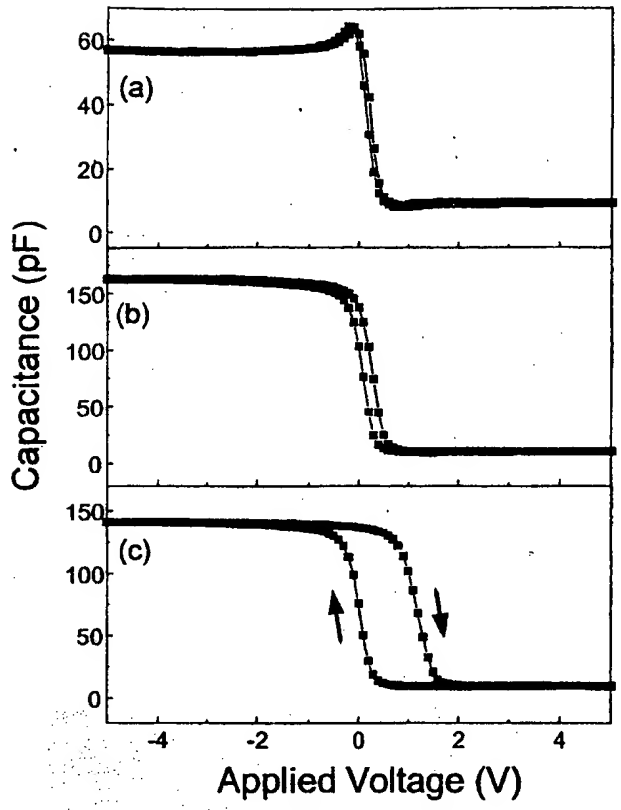

Fig. 5. C–V characteristics of Pt/STO(25 nm)/PZT(160 nm)/STO(25 nm)/Si structures annealed at 600°C (a) for 30 min, (b) for 1 h, and (c) annealed at 600°C for 1 h and post-annealed at 400°C for 30 min in oxygen ambient.

current density might result in decreasing the value of memory window. Therefore, in order to improve the electrical properties, the STO/PZT/STO/Si (IFIS) structures were annealed at 600°C for 1 h and the Pt/STO/PZT/STO/Si (MIFIS) structures were post-annealed at 400°C for 30 min in oxygen ambient. Fig. 7 shows the *C–V* curves of Pt/STO(25 nm)/PZT(160 nm)/STO(25 nm)/Si structure as a function of an applied voltage. The clockwise hysteresis curves of memory window were obtained and the value of memory window was increased as increasing an applied voltage. The values of memory window were, respectively, about 1.2 and 2 V at applied voltages of 5 and 7 V. The negative shift of flatband voltage was not observed at a high

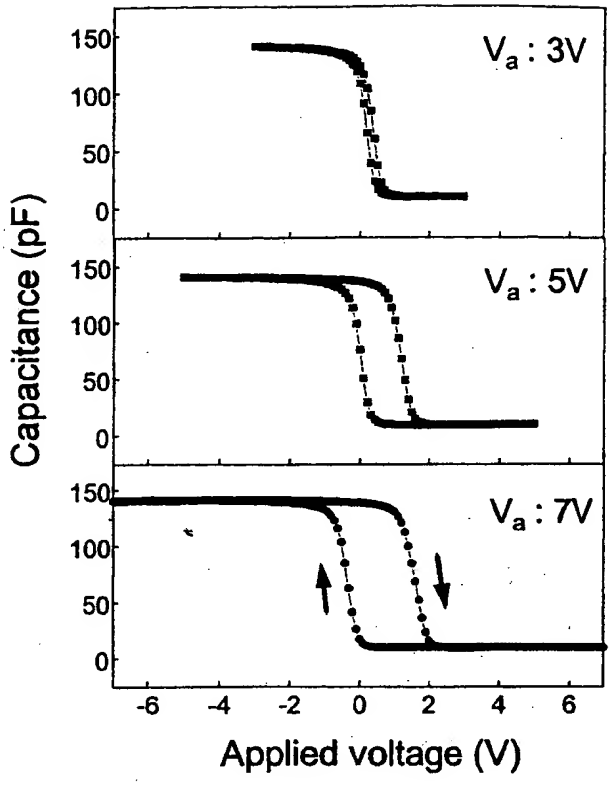

Fig. 7. C–V characteristics of Pt/STO(25 nm)/PZT(160 nm)/STO(25 nm)/Si structure annealed at 600°C for 1 h and post-annealed for 400°C for 30 min in oxygen ambient.

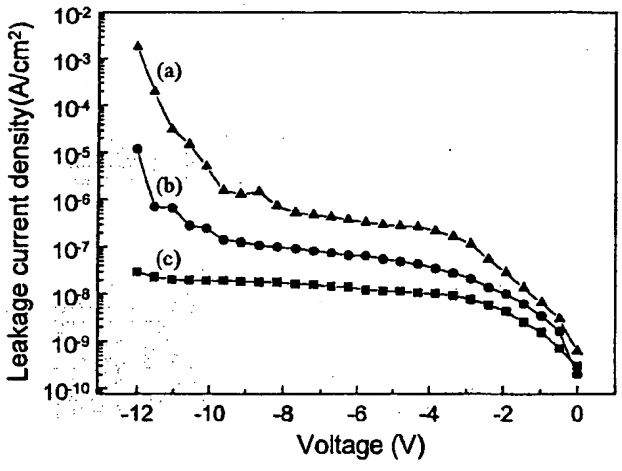

Fig. 6. Leakage current density of Pt/STO(25 nm)/PZT(160 nm)/STO(25 nm)/Si structures annealed at 600°C (a) for 30 min, (b) for 1 h, and (c) annealed at 600°C for 1 h and post-annealed at 400°C for 30 min in oxygen ambient.

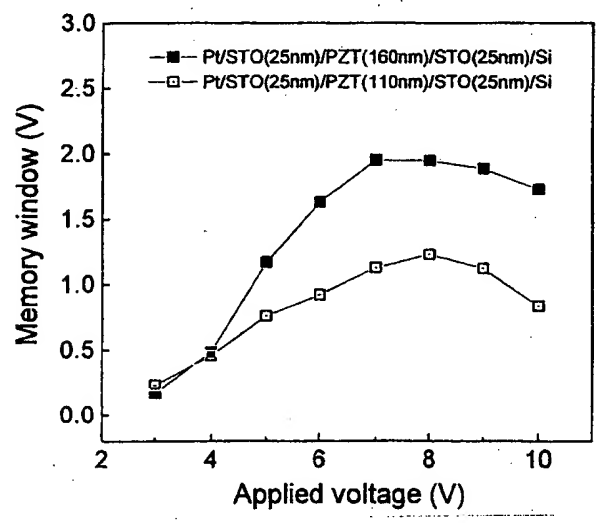

Fig. 8. Memory window vs. applied voltage of Pt/STO/PZT/STO/Si structures with a different thickness of PZT film.

applied voltage. Fig. 8 shows the plot of the memory window as a function of the applied voltage for the MIFIS structures with the 160 and 110 nm thickness of PZT films, respectively. The value of memory window was larger at the MIFIS structure with the 160 nm thickness of PZT film. This result might be induced by the division of the applied voltage, which was proportional to the inverse of the capacitance of each layer. The increase the thickness of PZT film caused a low applied voltage. A memory window could be directly obtained by the value of applied voltage, which is demanded in order to reverse the polarization direction of PZT film. Therefore, the low division of a applied voltage at PZT film might result in the increase of a applied voltage reversing the polarization direction of PZT film and then a memory window might be increased. However, the values of memory window were decreased above a critical applied voltage due to the charge injection into SiO_2 layer since a high electric field was applied at SiO_2 layer.

4. Conclusions

$Pt/SrTiO_3/Pb(Zr_{0.52},Ti_{0.48})O_3/SrTiO_3/Si$ (MIFIS) ferroelectric gate oxide structures were prepared by an r.f. sputtering method for the application of non-destructive read out ferroelectric RAM (NDRO-FRAM). The STO film was used as a buffer layer to prevent the interaction between the PZT film and the Si substrate and also between the PZT films and the Pt top electrodes. In the PZT/Si structure, a serious inter-diffusion of Pb atoms into the Si substrate was observed. However, the STO/PZT/STO/Si structure had a perfect perovskite PZT phase and a flat and clear interface without the inter-diffusion of Pb atoms. When the Pt/STO/PZT/STO/Si structures were post-annealed at 400°C for 30 min after depositing the Pt top electrodes, the leakage current density was decreased to about 10^{-8} A/cm^2. The memory window at the MIFIS structure might be increaesed by this improvement of a leakage current density. When the Pt/STO(25 nm)/PZT(160 nm)/STO(25 nm)/Si structures were annealed at 600°C for 1 h and post-annealed at 400°C for 30 min in oxygen ambient, the maximum value of memory window was 2 V at the applied voltage of 7 V. The memory window was decreased as decreasing the thickness of PZT film due to a lower voltage applied at the PZT film. Therefore, Pt/STO/PZT/STO/Si ferroelectric gate structures were promising for the application of NDRO-FRAMs.

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